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# [ACCESS METHOD AND ARCHITECTURE OF NON-VOLATILE RANDOM ACCESS MEMORY]

## Abstract

The present invention provides a method as well as anarchitecture for a host equipped with a CPU-level processing capability to access a Non-Volatile Random Access Memory (NVRAM) and at least a controller via a simple 3-wire/4-wire mechanism. The data stored in the NVRAM are shared with the controller and the host. More importantly, a multi-access mechanism further having a pragmatic bitdetermines the pragmatic bit for either the controller or the NVRAM. With the method of the present invention, computer system resources can be fully utilized, and thereby, peripheral devices can be easily added to the system in an inexpensive and highly efficient way.